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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,085	10/17/2003	Hiroshi Maeda	244081US2	9074

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,085	MAEDA, HIROSHI	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4* is/are rejected.

7)☒ Claim(s) *2,3 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-17-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 17 October 2003.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Flip Chip Mounting Method of Forming a Solder Bump on a Chip Pad that is Exposed Through an Opening Formed in a Polyimide Film that Includes Utilizing Underfill to Bond the Chip to a Substrate.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 includes step (f), which is performed after step (c), of using the polyimide film as a mask to selectively remove the nitride film portion of the insulation film from above the fuse. However, claim 4 contradicts claim 2, from which it depends, because claim 2 requires that the insulation film above the fuse is selectively removed from above the fuse as part of step (b) (see claim 2, lines 4-5) and step (b) must be performed before step (c) (i.e. before the formation of the polyimide film) as required by claim 1 (see claim 1, lines 4-5).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Takase et al. (US 6,028,011).

Referring to Figs. 8A-8E and column 10, line 26 to column 12, line 41, Takase et al. disclose a flip chip method that includes the following features:

- Pads comprising aluminum electrodes (47) and nickel-gold barriers (48) are formed on a silicon substrate (49);

- The pads (47/48) are covered with a first polyimide layer (50) (i.e. an insulation film) and openings are formed in the first polyimide layer (50) to expose the pads (47/48) as shown in Fig. 8B;
- Then a second polyimide film (51) is formed on the first polyimide layer (50) and openings are formed in the second polyimide layer (51) to expose the pads (47/48) as shown in Fig. 8C;
- The openings of the first polyimide film (50) and the second polyimide film (51) are filled with cream solder (52) as shown in Fig. 8D;
- Solder bumps (53) are then formed by reflowing the cream solder as shown in Fig. 8E; and
- The solder bumps (53) are subsequently flip chip bonded to a circuit substrate and sealed by underfilling with epoxy resin to form a semiconductor module as described in column 12, lines 37-41 (also see column 9, lines 52-67).

These are all of the limitations set forth in claim 1 of the applicant's invention.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateiwa (JP 2000-357743 A – from applicant's IDS) in view of Takase et al. (US 6,028,011).

As best understood by the examiner, claim 4 is being interpreted to mean that the selective removal of the insulation film from above the fuse does not have to be performed during step (b).

Referring to Figs. 2(a)-2(d) and the JPO abstract, Tateiwa discloses a method of manufacturing a semiconductor device that includes the following features:

- An uppermost metal interconnection layer corresponding to a semiconductor device is patterned to form a fuse (11) and a bonding pad (12);
- The fuse (11) and bonding pad (12) are sequentially covered with a TEOS film (13) (i.e. silicon oxide) and a silicon nitride film (14) as shown in Fig. 2(a);
- An opening (15) is formed through the TEOS (13) and silicon nitride (14) films to expose the bonding pad as shown in Fig. 2(b);
- A polyimide film (18) is then formed on the silicon nitride film (14) with openings (16, 17) formed over the fuse (11) and bonding pad (12), respectively, as shown in Fig. 2(c); and
- The silicon nitride (14) above the fuse (11) is selectively removed using the polyimide film (18) as a mask as shown in Fig. 2(d).

These are limitations set forth in claims 1, 4 of the applicant's invention.

However, Tateiwa lacks steps (d) and (e) as set forth in claim 1 of the applicant's invention, which are to form a solder bump on the pad (step (d)) and to bond the chip to a substrate using underfill (step(e)).

Takase et al. teach the formation of solder bumps (53) by filling openings formed in polyimide films (50, 51) with cream solder (52) and reflowing the cream solder (see Figs. 8D, 8E, and column 11, lines 6-13). The solder bumps (53) are subsequently flip chip bonded to a circuit substrate and sealed by underfilling with epoxy resin to form a semiconductor module (see column 9, lines 52-67 and column 12, lines 37-41).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings Tateiwa and Takase et al. in order to form a solder bump, for flip chip bonding with underfill to a substrate as taught by Takase et al., on the bond pad of Tateiwa. Takase et al. recognize that flip chip bonding has numerous advantages for mounting semiconductor devices including accurate positional alignment, reduced thickness, and high density mounting (see column 1, lines 24-32) and further that the use of underfill material seals the solder bumps (see column 9, lines 60-63), thereby protecting them from exposure to ambient conditions (e.g. moisture).

Allowable Subject Matter

8. Claims 2-3, 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: Claims 2-3, 5 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a flip chip mounting method that includes a chip with a pad and a fuse that are both covered with an insulation film combined with the step of selectively removing the insulation over the pad to expose the pad that also includes removing insulation above the fuse, wherein a polyimide film is formed on the insulation film with a first opening to expose the pad and a second opening above the fuse after the selectively removing step.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sakuyama et al. and Ho et al. teach methods of flip chip bonding to wiring boards that include underfilling.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot
Patent Examiner
Art Unit 2813